AMENDMENTS TO THE SPECIFICATION

Please replace the paragraphs beginning on page 17, line 1- page 19, line 5, with the following amended paragraphs:

Operation of the dual mode clock embodiment illustrated in Figure 5A can be understood by referring to the processing steps shown in the flowchart of Figure 11. In step 1102, the system enters the normal mode of operation wherein the oscillator 510 provides a clock signal directly to the baseband digital core 506 and to the frequency synthesizer 512 in the RF analog module 503 as discussed hereinabove. In step 1104, the status of the low-power mode signal, LPM, is inspected by the power management unit 408. If the LPM signal is low, processing returns to step 1102 wherein the normal mode of operation is continued. If, however, the test in step 1104 indicates that the LPM signal is high, processing proceeds to step 1106 where the transceiver 504 in the RF analog module 103 is turned off and the frequency synthesizer 512 is turned off in step 1108. In step 1110 the oscillator is switched to low-power mode and processing proceeds to step 1112 where the system is operating in low-power mode. In step 1114, a test is conducted to determine whether the state of the LPM signal has changed. If the test conducted in step 1114 indicates that the LPM signal remains high, processing returns to step 1112 and the system continues to operate in the low-power mode. If, however, the test conducted in step 1114 indicates that the LPM signal has transitioned from high to low, the system performs a power up sequence in step 1116 and processing returns to step 1102 wherein the system operates in a normal mode of operation.

Operation of the alternate embodiment of the dual mode clock illustrated in Figure 5B can be understood from the processing steps illustrated in the flowchart of Figure 12. In step 1202, the system enters the normal mode of operation wherein the oscillator 510 provides a clock signal directly to the baseband digital core 506 and to the frequency synthesizer 512 in the RF analog module 503 as discussed hereinabove. In step 1204, the status of the low-power mode signal LPM, is inspected by the power management unit 408. If the low-power mode signal is low, processing returns to step 1202 wherein the normal mode of operation is continued. If, however, the test in step 1204 indicates that the LPM signal is high, processing proceeds to step 1206 where the transceiver 504 in the RF analog module 503 is turned off. In step 1208 the oscillator is switched to low-power mode and processing proceeds to step 1210 where the system is operating in low-power mode. In step 1212, a test is conducted to determine whether the state

of the LPM signal has changed. If the test conducted in step 1212 indicates that the LPM signal remains high, processing returns to step 1210 and the system continues to operate in the low-power mode. If, however, the test conducted in step 1212 indicates that the low-power mode signal has transitioned from high to low, the system performs a power up sequence in step 1214 and processing returns to step 1202 wherein the system operates in a normal mode of operation.

Operation of the alternate embodiment of the dual mode clock illustrated in Figure 5C can be understood from the processing steps illustrated in the flowchart of Figure 13. In step 1302, the system enters the normal mode of operation wherein the oscillator 510 provides a clock signal directly to the baseband digital core 506 and to the frequency synthesizer 512 in the RF analog module 503 as discussed hereinabove. In step 1304, the status of the low-power mode, LPM, is inspected by the power management unit 408. If the LPM signal is low, processing returns to step 1302 wherein the normal mode of operation is continued. If, however, the test in step 1304 indicates that the LPM signal is high, processing proceeds to step 1306 where the transceiver 504 in the RF analog module 503 is turned off. In step 1308 the oscillator is switched to low-power mode and processing proceeds to step 1310 where the oscillator operates as the source for the baseband clock. The frequency synthesizer 512 is turned off in step 1312 and processing proceeds to step 1314 where the system is operating in low-power mode. In step 1316, a test is conducted to determine whether the state of the LPM signal has changed. If the test conducted in step 1316 indicates that the LPM signal remains high, processing returns to step 1314 and the system continues to operate in the low-power mode. If, however, the test conducted in step 1316 indicates that the low-power mode signal has transitioned from high to low, the system performs a power up sequence in step 1318 and processing returns to step 1302 wherein the system operates in a normal mode of operation.